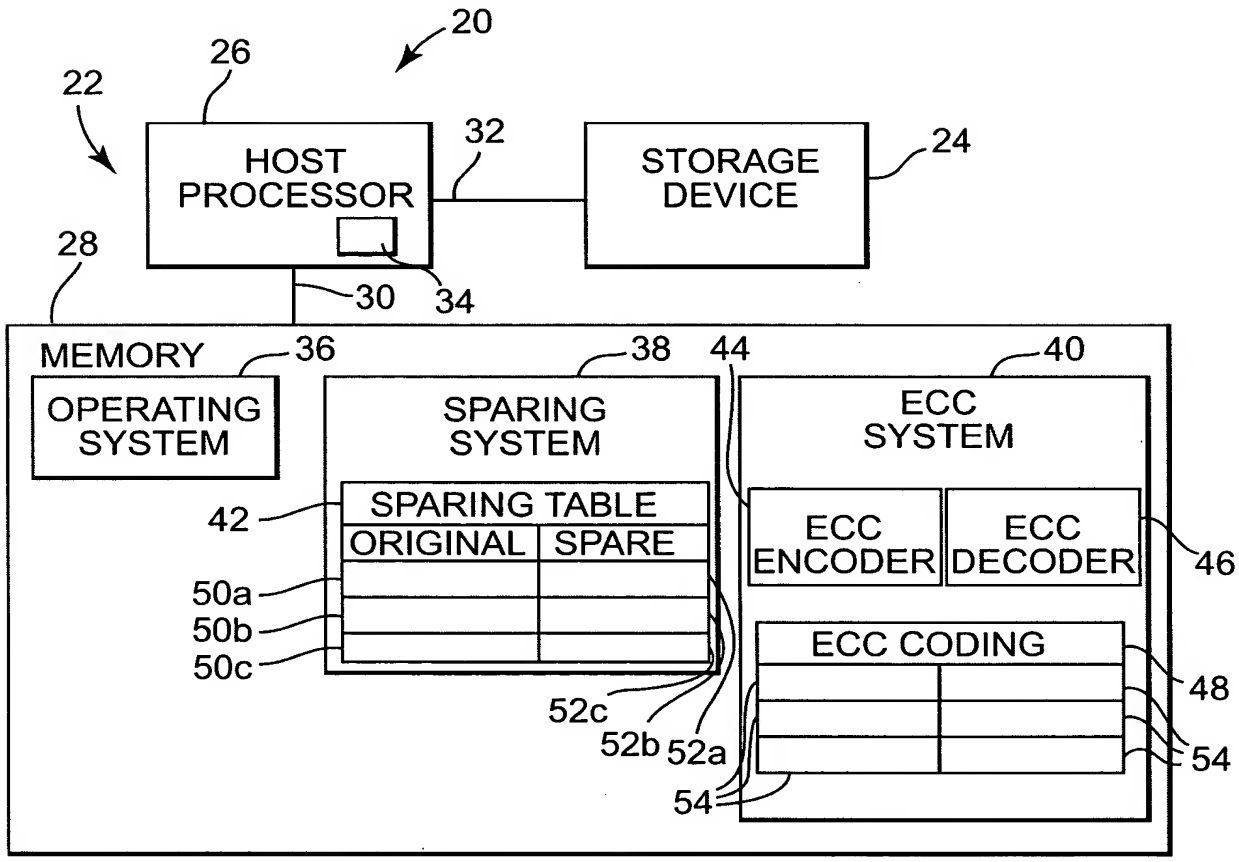
20
26
22
HOST PROCESSOR
32
STORAGE DEVICE
24
28
30
34
MEMORY
36
38
44
40
OPERATING SYSTEM
SPARING SYSTEM
ECC SYSTEM
SPARING TABLE
ORIGINAL
SPARE
42
ECC ENCODER
ECC DECODER
46
50a
50b
50c
ECC CODING
48
52c
52b
52a
54
54

Fig. 1

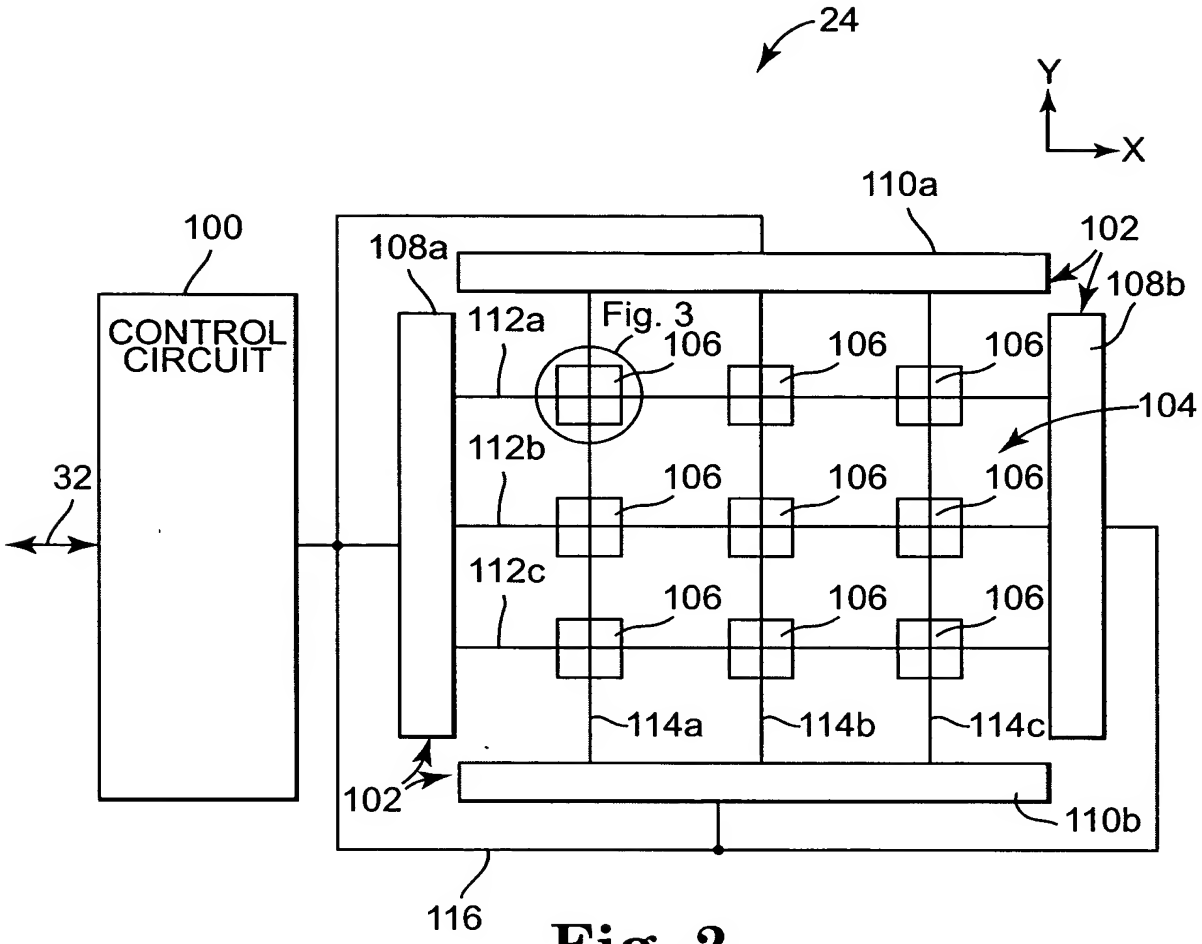
24
Y
X
110a
100
102
108a
108b
CONTROL CIRCUIT
112a
Fig. 3
106
104
112b
32
112c
114a
114b
114c
102
110b
116

Fig. 2

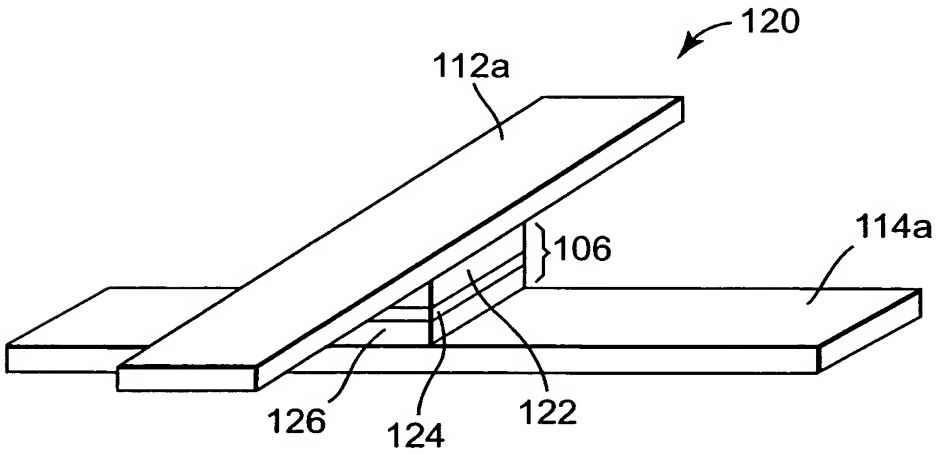
120
112a
106
114a
126
124
122

Fig. 3

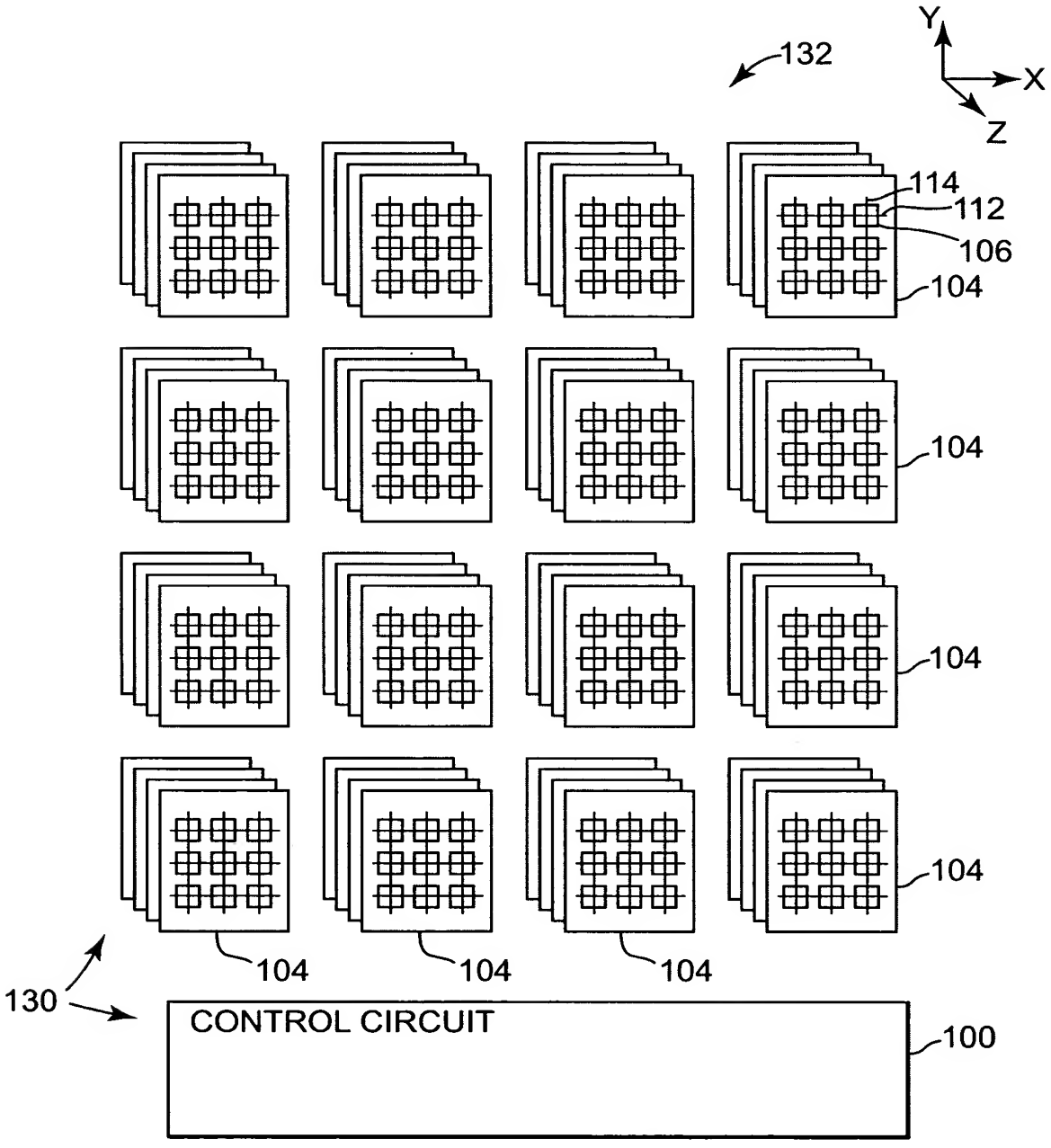
132
Y
X
Z
114
112
106
104
104
104
104
104
104
104
130
CONTROL CIRCUIT
100

Fig. 4

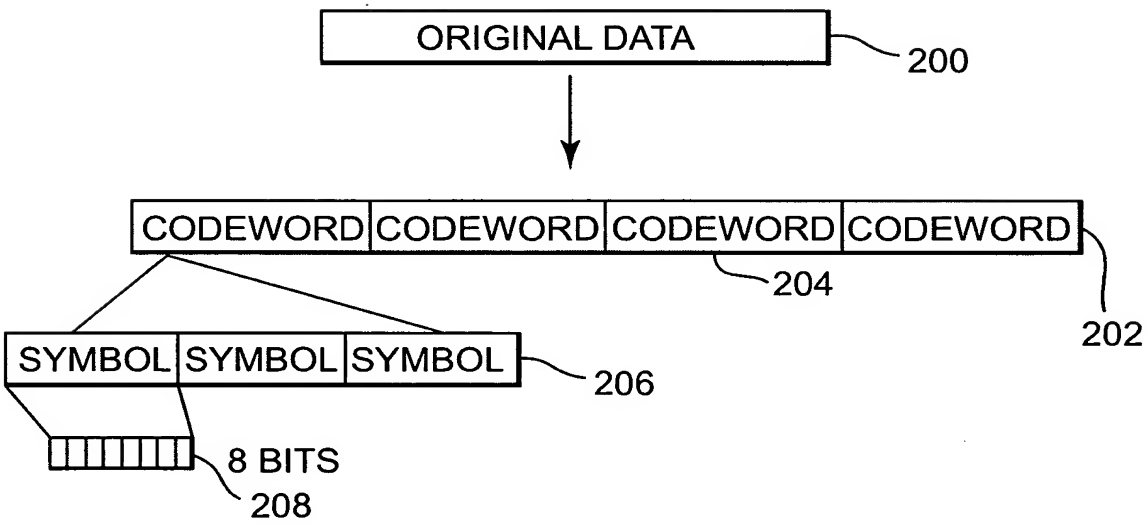
ORIGINAL DATA
200
CODEWORD
CODEWORD
CODEWORD
CODEWORD
204
202
SYMBOL
SYMBOL
SYMBOL
206
8 BITS
208

Fig. 5

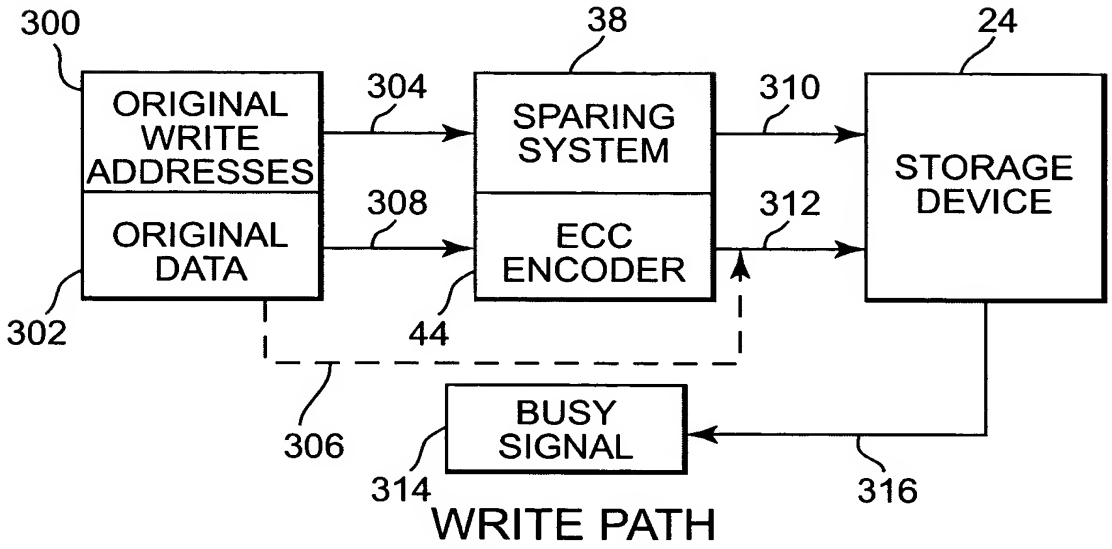
300
38
24
ORIGINAL WRITE ADDRESSES
304
SPARING SYSTEM
310
STORAGE DEVICE
ORIGINAL DATA
308
ECC ENCODER
312
302
44
306
BUSY SIGNAL
314
316
WRITE PATH

Fig. 6A

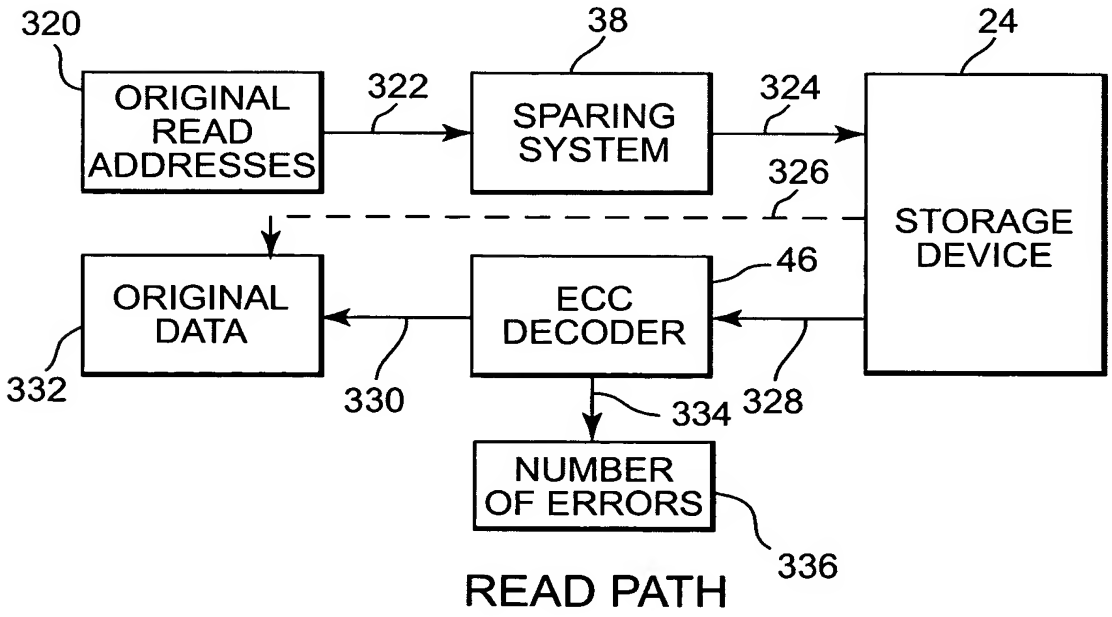
320
38
24
ORIGINAL READ ADDRESSES
322
SPARING SYSTEM
324
326
STORAGE DEVICE
46
ORIGINAL DATA
ECC DECODER
332
330
328
334
NUMBER OF ERRORS
336
READ PATH

Fig. 6B

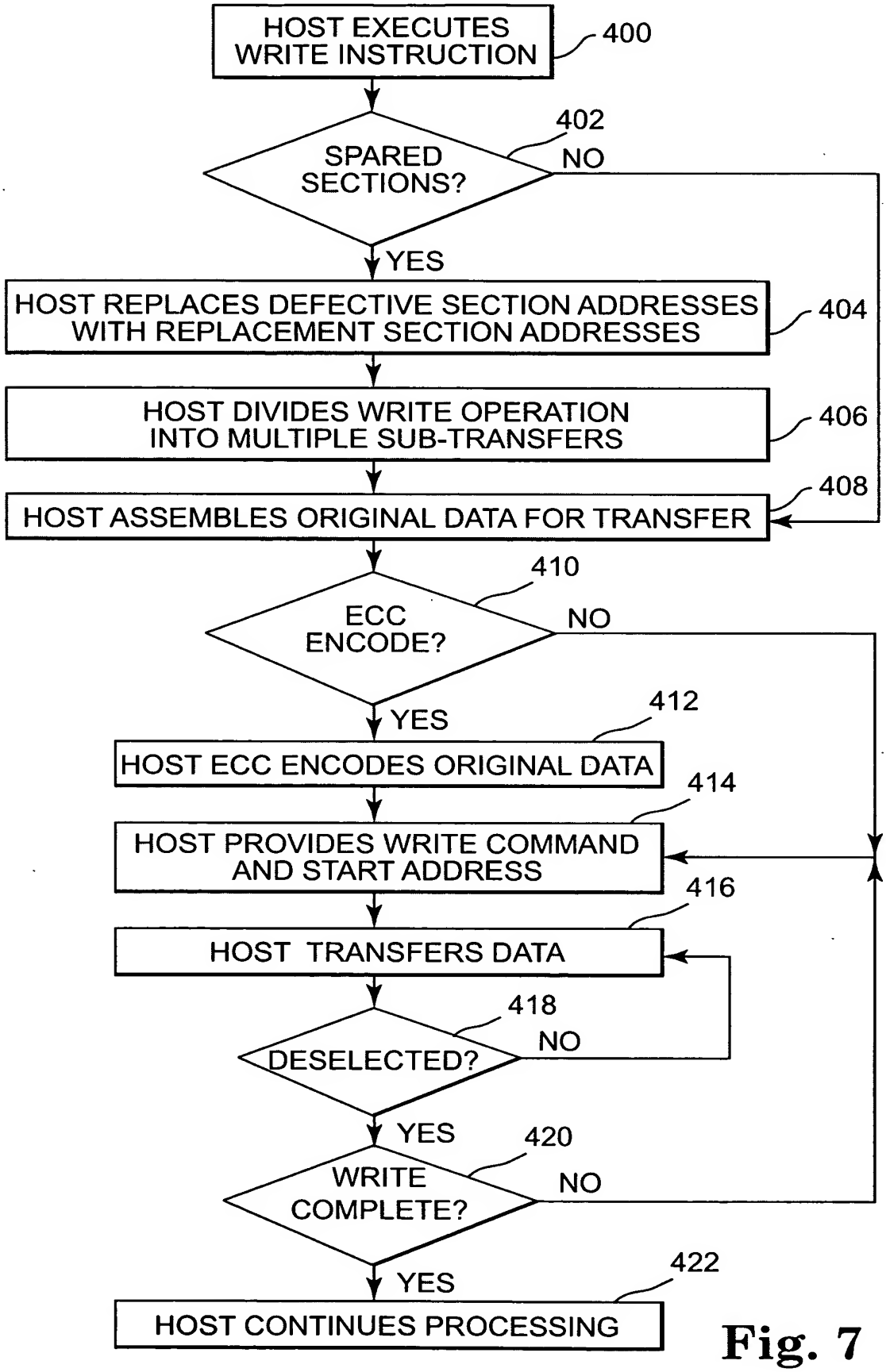
HOST EXECUTES WRITE INSTRUCTION
400
SPARED SECTIONS?
402
NO
YES
HOST REPLACES DEFECTIVE SECTION ADDRESSES WITH REPLACEMENT SECTION ADDRESSES
404
HOST DIVIDES WRITE OPERATION INTO MULTIPLE SUB-TRANSFERS
406
HOST ASSEMBLES ORIGINAL DATA FOR TRANSFER
408
ECC ENCODE?
410
NO
YES
HOST ECC ENCODES ORIGINAL DATA
412
HOST PROVIDES WRITE COMMAND AND START ADDRESS
414
HOST TRANSFERS DATA
416
DESELECTED?
418
NO
YES
WRITE COMPLETE?
420
NO
YES
HOST CONTINUES PROCESSING
422

Fig. 7

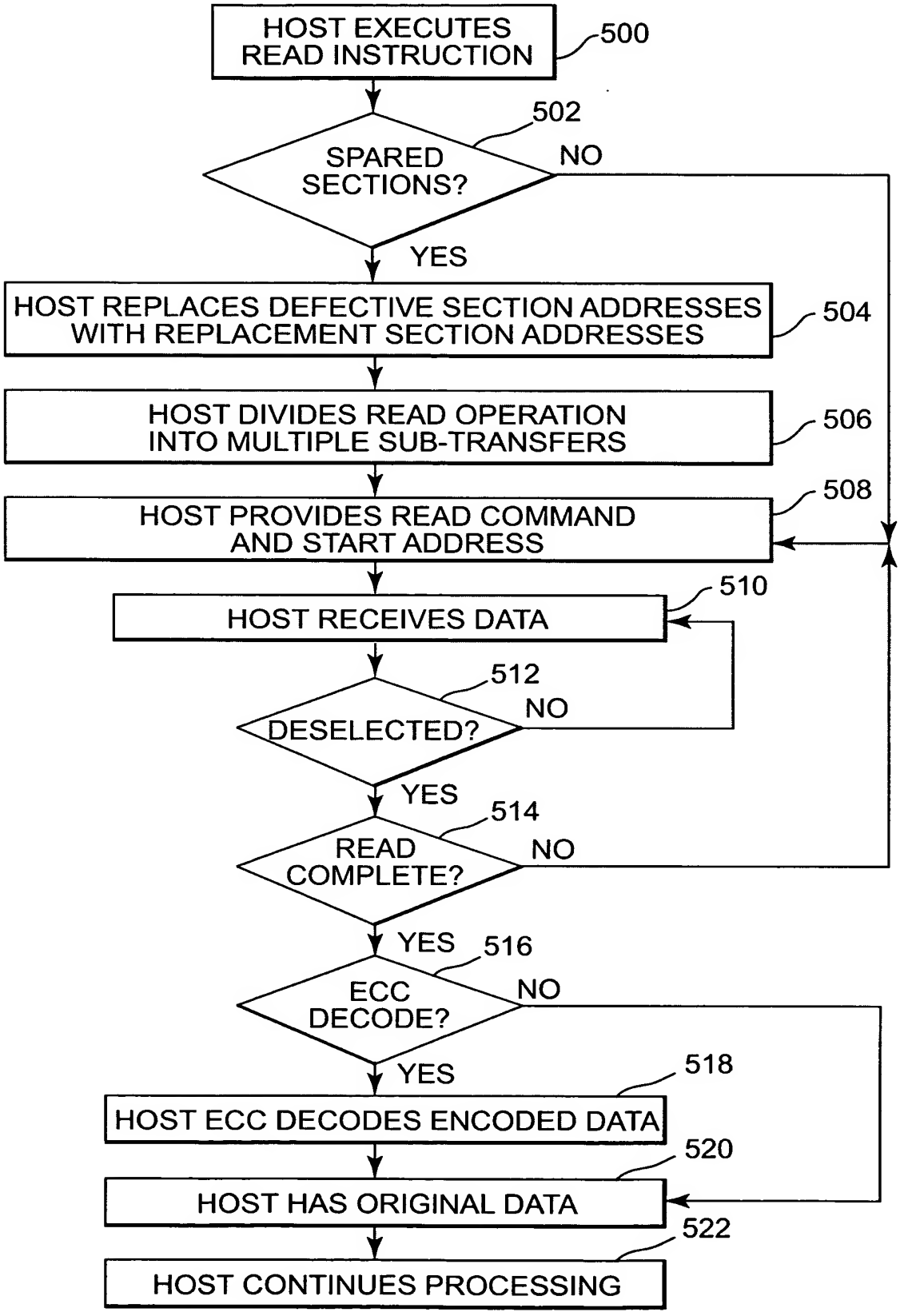
HOST EXECUTES READ INSTRUCTION
500
502
SPARED SECTIONS?
NO
YES
HOST REPLACES DEFECTIVE SECTION ADDRESSES WITH REPLACEMENT SECTION ADDRESSES
504
HOST DIVIDES READ OPERATION INTO MULTIPLE SUB-TRANSFERS
506
HOST PROVIDES READ COMMAND AND START ADDRESS
508
HOST RECEIVES DATA
510
512
DESELECTED?
NO
YES
514
READ COMPLETE?
NO
YES
516
ECC DECODE?
NO
YES
518
HOST ECC DECODES ENCODED DATA
520
HOST HAS ORIGINAL DATA
522
HOST CONTINUES PROCESSING

Fig. 8